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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/674,197	09/29/2003	Huo-Yuan Lin	DEE-PT131	2674

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EXAMINER	
RIAD, AMINE	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 04/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/674,197	LIN, HUO-YUAN	
	Examiner	Art Unit	
	Amine Riad	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Sept.29,2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *Sept.29,2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892) AP.
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date, _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-22 have been presented for examination.

Claims 1-22 have been rejected.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 6-15, and 17-22 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Noll et al. (U.S. Patent No. 5,835,695).

In regard to claim 1,

Noll discloses a method for recovering a basic input/output system (BIOS) memory circuit in a computer system, comprising steps of:

- Providing a memory device comprising a first basic input/output system memory circuit (Figure 1; item 22 BIOSROM 1) and a second basic input/output system memory circuit (Figure 1; item 30 BIOSROM 2),

- First basic input/output system memory circuit and said second basic input/output system memory circuit respectively having a first computer program and a second computer program stored therein, wherein said first basic input/output system memory circuit and said second basic input/output system memory circuit

are employed to initiate an operation of said computer system; (Column 1; lines 49-54)

- Enabling said second basic input/output system memory circuit upon booting said computer system; (Column 3; lines 43-47 [Since the computer did not initialize with the first BIOS this phase of no initialization is still considered as booting])
- Detecting if said first computer program includes an error; (Column 1; line 65-67) and (Column 2; lines1-2)
- Re-programming said first basic input/output system memory circuit based on said second computer program when said error is detected in said first computer program. (Column 2; lines 16-20)

In regard to claims 2 and 13,

Noll discloses a method according to claim 1 wherein said first computer program and said second computer program are identical. (Column 1; lines 63-65)

In regard to claims 3 and 14,

Noll discloses a method according to claim 1 wherein said first computer program and said second computer program are different. (Column 1; line 63-65 [Noll discloses that first BIOS and second BIOS contain preferably identical program instructions. This inherently suggests that first BIOS and second BIOS could contain different program instructions])

In regard to claims 4 and 15,

Noll discloses a method according to claim 1 wherein said enabling step further comprises steps of:

- Providing a chip enabling circuit having a chip enabling control terminal;(Figure 1; item 36 Chip enable circuit)
- Enabling said second BIOS memory circuit through said chip enabling control terminal of said chip enabling circuit upon booting said computer system.(Column 3;lines 24-26)

In regard to claims 6 and 17,

Noll discloses a method according to claim 1 wherein said detecting step further comprises steps of:

- Providing an error-detecting circuit; (Figure 1; item 54)
- Checking an error-detecting data value contained in said first computer program through said error-detecting circuit for determining if said first computer program includes said error. (Column 7; lines 56-59) [This part of the reference discloses that the error detection circuit includes computer instructions that are executed by the CPU] and (Column 7; lines 1-3) [this part of the reference discloses that the CPU 12 checks through the error detection circuit instructions to determine whether or not the first BIOS contains data errors]

In regard to claims 7 and 18,

Noll discloses a method according to claim 6 wherein said error-detecting data value is a checksum data value. (Column 4; lines 26-28)

In regard to claims 8 and 19,

Noll discloses a method according to claim 6 wherein said error-detecting data value is a parity check data value. (Column 4; line (30-31) [use of other error detection techniques are well known to those of ordinary skill in the art is interpreted as error-detecting data value is a parity check data value])

In regard to claim 9 and 20

Noll discloses a method according to claim 6 wherein said error-detecting data value is a cyclic redundancy check (CRC) data value. (Column 4; lines 28-30)

In regard to claims 10 and 21,

Noll discloses a method according to claim 1 wherein said first basic input/output system memory circuit further comprises a flash utility for reprogramming said first basic input/output system memory circuit based on said second computer program. (Column 3; lines 62-65)

In regard to claims 11 and 22,

Noll discloses a method according to claim 1 wherein said second basic input/output system memory circuit further comprises a flash utility for reprogramming said first basic

input/output system memory circuit based on said second computer program. (Column 3; lines 16-17 [In this part Noll discloses that First BIOS is similar to the Second BIOS]) and (Column 3; lines 62-65[Since the First BIOS is similar to the Second BIOS, and the first one contains a flash utility than the second one does also])

In regard to claim 12,

Noll discloses a method for initiating a computer system, comprising steps of:

- Providing a memory chip comprising a first basic input/output system memory circuit (Figure 1; item 22 BIOSROM 1) and a second basic input/output system memory circuit (Figure 1; item 30 BIOSROM 2),
- First basic input/output system memory circuit and said second basic input/output system memory circuit respectively having a first computer program and a second computer program stored therein, wherein said first basic input/output system memory circuit and said second basic input/output system memory circuit are employed to initiate an operation of said computer system; (Column 1; lines 49-54)
- Enabling said second basic input/output system memory circuit upon booting said computer system; detecting if said first computer program includes an error; (Column 3; lines 43-47 [Since the computer did not initialize with the first BIOS this phase of no initialization is still considered as booting])

- Re-programming said first basic input/output system memory circuit based on said second computer program when said error is detected in said first computer program;(Column 2; lines 18-20 " the first BIOS memory may be reprogrammed using the computer program instructions stored within the second BIOS memory")

- Enabling said first basic input/output system memory circuit and disabling said second basic input/output system memory circuit; (Column 7; line 36-38 [Following the reprogramming of the first BIOS the computer continues the BIOS shadowing process this is interpreted as the first BIOS is enabled])

- Initiating an operation of said computer system through said first basic input/output system memory circuit.(Column 7; line 38-39 [CPU boots the system after finishing the shadowing process from BIOS one])

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noll et al. (U.S. Patent No. 5,835,695) in view of Chang et al. (Patent Application Publication No. 2004/0111633).

Noll discloses a method for recovering a basic input/output system, substantially as specified in parent claims 4 and 15.

Noll does not disclose that the enabling control terminal is a general-purpose input/output pin (GPIO pin)

Chang teaches BIOS control terminal implemented using a general-purpose input/output pin (GPIO pin). (Page 1; Paragraph 7)

It would have been obvious to one of ordinary skill in the art at the time the invention to implement the enabling control terminal of Noll using a GPIO pin, as suggested by Chang.

One of ordinary skill in the art would have been motivated to use a GPIO pin because GPIO pin has the advantage of reducing the components since it is directly coupled to the BIOS.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S patent 6,934,873 teaches most of the limitations, but instead of including a second BIOS the reference has a second node, on the other hand patent application publication contains some elements, but lacks important element, which is that both first and second BIOS are located on the same computer system. See PTO 892.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amine Riad whose telephone number is 571-272-8185. The examiner can normally be reached on 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on 571-272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S patent 6,34,873 teaches most of the limitations, but lacks switching modes, on the other hand U.S. patent 5,805,882 contains some elements, but lacks important element, which are first and second bridge. See PTO 892.d from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AR
Patent Examiner

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